WHAT IS CLAIMED IS:

1. A circuit comprising:

a static low-swing driver circuit to receive a full-swing input signal, to convert the full-swing input signal to a low-swing signal, and to transmit the low-swing signal; and

a dynamic receiver circuit to receive the low-swing signal and to convert the low-swing signal to a full-swing signal.

2. A circuit according to Claim 1, further comprising:

an interconnect coupled to the driver circuit and to the receiver circuit, the interconnect to receive the low-swing signal from the driver circuit and to transmit the low-swing signal to the receiver circuit,

wherein the interconnect does not comprise a repeater.

3. A circuit according to Claim 1, wherein the driver circuit comprises:

an input line to receive the full-swing input signal;

an inverter coupled to a supply voltage, the input line coupled to an input of the inverter;

a delay element coupled to the supply voltage, the input line coupled to an input of the delay element, and a propagation delay associated with the delay element matching a propagation delay associated with the inverter;

a first transistor, a gate of the first transistor coupled to an output of the inverter and a drain of the transistor coupled to a first voltage, the first voltage less than the supply voltage;

a second transistor, a gate of the second transistor coupled to an output of the delay element and a drain of the second transistor coupled to a source of the first transistor at an output node; and

an output line coupled to the output node, the output line to transmit the low-swing signal.

4. A circuit according to Claim 1, wherein the receiver circuit comprises a positive edge-triggered dynamic sense-amplifying flip-flop.

5. A circuit according to Claim 4, wherein the driver circuit comprises:

a driver input line to receive the full-swing input signal;

an inverter coupled to a supply voltage, the input line coupled to an input of the inverter;

a delay element coupled to the supply voltage, the input line coupled to an input of the delay element, and a propagation delay associated with the delay element matching a propagation delay associated with the inverter;

a first transistor, a gate of the first transistor coupled to an output of the inverter and a drain of the transistor coupled to a first voltage, the first voltage less than the supply voltage;

a second transistor, a gate of the second transistor coupled to an output of the delay element and a drain of the second transistor coupled to a source of the first transistor at an output node; and

a driver output line coupled to the output node, the output line to transmit the low-swing signal.

6. A circuit according to Claim 1, wherein the receiver circuit comprises a true single phase clock-style positive edge-triggered level-restoring flip-flop.

7. A circuit according to Claim 6, wherein the receiver circuit comprises:

an input line to receive the low-swing signal;

an inverter coupled to V_{ss} and to a first voltage less than V_{cc}, the inverter coupled to a clock signal to control signal propagation through the inverter an input of the inverter coupled to the input line;

a pull-up transistor coupled an output of the inverter and to V_{cc};

8. A circuit according to Claim 7, wherein the driver circuit comprises:

an input line to receive the full-swing input signal;

an inverter coupled to a supply voltage, the input line coupled to an input of the inverter;

a delay element coupled to the supply voltage, the input line coupled to an input of the delay element, and a propagation delay associated with the delay element matching a propagation delay associated with the inverter;

a first transistor, a gate of the first transistor coupled to an output of the inverter and a drain of the transistor coupled to a first voltage, the first voltage less than the supply voltage;

a second transistor, a gate of the second transistor coupled to an output of the delay element and a drain of the second transistor coupled to a source of the first transistor at an output node; and

an output line coupled to the output node, the output line to transmit the low-swing signal.

9. A driver circuit comprising:

a driver input line to receive the full-swing input signal;

an inverter coupled to a supply voltage, the input line coupled to an input of the inverter;

a delay element coupled to the supply voltage, the input line coupled to an input of the delay element, and a propagation delay associated with the delay element matching a propagation delay associated with the inverter;

a first transistor, a gate of the first transistor coupled to an output of the inverter and a drain of the transistor coupled to a first voltage, the first voltage less than the supply voltage;

a second transistor, a gate of the second transistor coupled to an output of the delay element and a drain of the second transistor coupled to a source of the first transistor at an output node; and

a driver output line coupled to the output node, the output line to transmit the low-swing signal.

10. A circuit according to Claim 9, further comprising:

an interconnect coupled to the driver output line, the interconnect to receive the low-swing signal from the driver circuit and to transmit the low-swing signal to a receiver circuit.

wherein the interconnect does not comprise a repeater.

11. A system comprising:

a microprocessor comprising:

a static low-swing driver circuit to receive a full-swing input signal, to convert the full-swing input signal to a low-swing signal, and to transmit the low-swing signal; and

a dynamic receiver circuit to receive the low-swing signal and to convert the low-swing signal to a full-swing signal; and

a double data rate memory coupled to the microprocessor.

12. A system according to Claim 11, the microprocessor further comprising:

an interconnect coupled to the driver circuit and to the receiver circuit, the interconnect to receive the low-swing signal from the driver circuit and to transmit the low-swing signal to the receiver circuit,

wherein the interconnect does not comprise a repeater.

13. A system according to Claim 11, wherein the driver circuit comprises:

an input line to receive the full-swing input signal;

an inverter coupled to a supply voltage, the input line coupled to an input of the inverter;

a delay element coupled to the supply voltage, the input line coupled to an input of the delay element, and a propagation delay associated with the delay element matching a propagation delay associated with the inverter;

a first transistor, a gate of the first transistor coupled to an output of the inverter and a drain of the transistor coupled to a first voltage, the first voltage less than the supply voltage;

a second transistor, a gate of the second transistor coupled to an output of the delay element and a drain of the second transistor coupled to a source of the first transistor at an output node; and

an output line coupled to the output node, the output line to transmit the low-swing signal.

14. A system according to Claim 11, wherein the receiver circuit comprises a positive edge-triggered dynamic sense-amplifying flip-flop.

15. A system according to Claim 11, wherein the receiver circuit comprises a true single phase clock-style positive edge-triggered level-restoring flip-flop.